

### REQUEST FOR ACTION (RFA) RESPONSE

### GLAST LAT Project Calorimeter Peer Review

17 – 18 March 2003

Action Item:	CAL – 009
<b>Presentation Section:</b>	Thermal
Submitted by:	Tom McCarthy

**Request:** Parts thermal analysis - Update Board level analyses using vacuum

rated parts parameter, i.e., theta-jc, theta-cl, etc.

Reason / Board level analysis used theta-ja to tie component to board. The use of theta-ja an ambient part parameter, to represent the part in vacuum

of theta-ja, an ambient part parameter, to represent the part in vacuum may not be conservative. For vacuum/space application analysis, each part must be considered using theta-jc and how is part tied to board,

i.e., through lead and/or is it bonded?

#### Response: 18 April 2003

Analysis was rerun using the theta-jb (junction to board), which accounted for theta-jc (junction to case) and theta-cb (case to board).

The attached view graph corrects the board level thermal analysis summary that was presented at the Peer Review (page 7-38) to address the request of this RFA.

The AFEE Thermal Study report will be updated to add this information.



## **AFEE Thermal Analysis**

- AFEE Thermal Analysis Summary. Dated 4/03 Author Peck Sohn, Swales **Aerospace**
- Table of maximum silicon die temperature for 25 C Base Plate temperature

Device	GCRC	GCFE	ADC	DAC	Ref.
Die Junction Temp. Degrees C	36.7	33.5	33.8	33.8	35.1

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Analysis result, Calorimeter AFEE electronics do not have any thermal problems Assumptions

28.3	30.1		28.0
29.5	32.4	Modeled AFEE Board	29.0
29.7	33.3	Temperature, Degree C,	29.1
28.9	31.8	for 25 C Base Plate Temp.	28.4
26.8	29.1		26.6

	Modeled Heat Dissipation	Theta Junction to Board (C/W)			
GCRC	65 mW	50			
GCFE	11.5 mW	114			
ADC	2 mW	183			
DAC	4 mW	86			
Ref.	7 mW	232			
Total Power per AFEE	952 mW				

AFEE PCB, Qty 2 of 1.4 mil thick Copper Thermal Plane Layers. Naval Research Lab

Washington DC



# **AFEE Thermal Analysis**

- ☐ AFEE Thermal Analysis Summary. Dated 4/03 Author Peck Sohn, Swales Aerospace
- □ Table of maximum silicon die temperature for 50 C Base Plate temperature

Device	GCRC	GCFE	ADC	DAC	Ref.
Die Junction Temp. Degrees C	61.3	58.2	58.5	58.4	59.7

Analysis result, Calorimeter AFEE electronics do not have any thermal problems

53.2	55.0		53.0
54.3	57.1	Modeled AFEE Board	53.9
54.5	57.9	Temperature, Degree C, for	53.9
53.7	56.5	50 C Base Plate Temp.	53.2
51.7	53.9		51.5



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